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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Jun KANAMORI

Group Art Unit: 2814

Continued Prosecution Application of
Serial No.: 09/398,189

Examiner: S. Rao

#14/C
7-19-01
Payton

Filed: September 17, 1999

For: METHOD OF FABRICATING A SEMICONDUCTOR DEVICE WITH SELF-ALIGNED SILICIDE AREAS FORMED USING A SUPPLEMENTAL SILICON OVERLAYER

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Date: July 12, 2001

Sir:

Preliminary to the examination of the present Continued Prosecution Application, please enter the following amendments and remarks.

In the Claims:

Please add new claims 23 and 24 as follows:

~~-23. A method for fabricating a semiconductor device, comprising:~~

Dub DD

providing a semiconductor substrate which has a silicon region located on a insulating layer formed in the semiconductor substrate;

C1

forming a metal layer on the silicon region;

performing a first annealing to form a first-reacted silicide region;

forming a supplemental silicon layer on the first-reacted silicide region; and